Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of forming bit lines and bit line contacts of a memory device, comprising the steps of:
providing a substrate having a plurality of gate structures thereon, wherein each gate structure comprises a gate dielectric layer, a gate conductive layer and a cap layer, and wherein a spacer is formed on each sidewall of the gate structure;
forming a conductive layer over the substrate to cover the gate structures;
planarizing the conductive layer until the cap layer of the gate structures is exposed;
removing a portion of the conductive layer but retaining the conductive layer between neighboring gate structures to form a bit line contact;
forming a dielectric layer over the substrate to cover the gate structures and the bit line contact;
planarizing the dielectric layer the cap layer of the gate structures and the bit line contact is exposed; and
forming a bit line over the dielectric layer, wherein the bit line and the bit line contact are electrically connected.

[c2] 2. The method of claim 1, wherein before forming the bit

line over the dielectric layer, further comprises forming a stop layer over the dielectric layer such that the the bit line contact remain exposed.

[c3] 3. The method of claim 1, wherein before forming the conductive layer over the substrate, further comprises:
forming a barrier layer over the substrate and the gate structures; and
removing the barrier layer between two neighboring gate structures to expose the substrate.

[c4] 4. The method of claim 1, wherein the step of forming the bit line over the dielectric layer comprises:
forming a first dielectric layer over the dielectric layer;
forming a trench in the first dielectric layer such that the trench exposes the bit line contact; and
depositing conductive material into the trench to form the bit line.

[c5] 5. The method of claim 1, wherein the step of planarizing the conductive layer comprises performing a chemical mechanical polishing operation.

[c6] 6. The method of claim 1, wherein the step of planarizing the dielectric layer comprises performing a chemical mechanical polishing operation.

[c7] 7. The method of claim 1, wherein a width of the bit line

contact is substantially identical to a width of the bit line.

[c8] 8. The method of claim 1, wherein material constituting the bit line contact comprises doped polysilicon.

[c9] 9. The method of claim 1, wherein material constituting the bit line comprises tungsten.

[c10] 10. A method of forming a memory device, comprising the steps of:
providing a substrate comprising a memory cell region and a peripheral circuit region;
forming a plurality of gate structures over the substrate within the memory cell region, wherein each gate structure comprises a gate dielectric layer, a gate conductive layer and a cap layer, and wherein a spacer is formed on each sidewall of the gate structures;
forming a conductive layer over the substrate to cover the gate structures;
planarizing the conductive layer until the cap layer of the gate structures is exposed;
removing a portion of the conductive layer but retaining the conductive layer between two neighboring gate structures to form a bit line contact;
forming a dielectric layer over the substrate to cover the gate structures and the bit line contact;
planarizing the dielectric layer until the cap layer of the

gate structures and the bit line contact is exposed; and forming a bit line over the dielectric layer so that a contact is also formed within the dielectric layer in the peripheral circuit region, wherein the bit line is electrically connected to both the bit line contact and the contact.

[c11] 11. The method of claim 10, wherein before forming the bit line over the dielectric layer, further comprises forming a stop layer over the dielectric layer such that the stop layer exposes the bit line contact.

[c12] 12. The method of claim 10, wherein before the step of forming the conductive layer over the substrate, further comprises:
forming a barrier layer over the substrate and the gate structures; and
removing the barrier layer between two neighboring gate structures to expose the substrate.

[c13] 13. The method of claim 10, wherein the step of planarizing the conductive layer comprises performing a chemical mechanical polishing operation.

[c14] 14. The method of claim 10, wherein the step of planarizing the dielectric layer comprises performing a chemical mechanical polishing operation.

[c15] 15. The method of claim 10, wherein the bit line contact

has a width almost identical to the bit line.

[c16] 16. The method of claim 10, wherein the step for forming the bit line and the contact comprises:
forming a first dielectric layer over the substrate to cover the dielectric layer, the bit line contact and the gate structures;
forming a trench in the first dielectric layer such that the trench exposes the bit line contact;
forming an opening in the dielectric layer at the bottom of the trench within the peripheral circuit region, wherein the opening exposes the substrate; and
depositing conductive material into the trench and the opening to form a bit line and a contact.

[c17] 17. The method of claim 10, wherein material constituting the bit line contact comprises doped polysilicon.

[c18] 18. The method of claim 10, wherein material constituting the bit line comprises tungsten.